Reliability Evaluation of MIT/LL FDSOI 0.25 μm Process for Space Applications

(Part II)

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1.0 Introduction

The previous report titled, "Reliability Evaluation of Fully Depleted SOI (FDSOI) Technology for Space Applications," posted on the NEPP web site, provided a general overview of SOI technology including materials, process, reliability issues, and MIT/LL FDSOI processes and associated reliability test structures. The hot carrier degradation effects in the MIL/LL FDSOI FETs at $V_g = V_d/2$ conditions, which are known to maximize the interface trap generation have been investigated at JPL [1].

This report (Part II) of the continuing evaluation, addresses characterization of the N- and P-channel transistors, including scaling effects and estimation of the reproducibility of the front- and back-channel parameters was performed. The transistor measurements included threshold voltage, subthreshold slope, mobility of charge carriers, gate leakage currents, and investigation of the edge effects. Radiation effects and charge instability in FD SOIFETs will be discussed in part III of the report.

2.0 FDSOI Process Monitor Transistors

A detailed description of the test structures used in MIT/LL to control manufacturing process and, in particular, FDSOI FETs was provided in the previous report [2]. For this evaluation, four process monitor dice were received, containing NMOS/PMOS transistors of various sizes. There were 40 FETs in each dice with L = 0.2 μm to 0.8 μ and W = 0.5 μm to 100 μm.

The transistor structures were mesa-isolated and fabricated in SIMOX (separation by implantation of oxygen) wafers with silicon thickness 47 nm. The thickness of buried and thermal oxides was 170 nm and 7.3 nm. Polysilicon gates (200 nm of thickness) and active areas of the transistors were silicided after spacer formation.

3.0 FDSOI PM Parametric Measurements

The process monitor transistor characteristics were measured under probes using a Hewlett Packard Precision Semiconductor Analyzer (Model 4156A). Due to a strong coupling effect, characteristics of the front-channel transistors strongly depend on the voltage applied to the back gate and vice versa.

To characterize the gate oxide SOI and buried oxide SOI interfaces separately, the measurements were performed at "decoupling conditions" by biasing the opposite gate to create accumulation in the corresponding channel. The front gate characteristics were

measured at +10 V on the back gate for N-channel transistors and –10V for the P-channel transistors. The back gate characteristics were measured at ± 1 V correspondingly for N- and P-channel transistors.

The threshold voltage, V_{th}, was measured using two methods: at the constant current level ($I_d = I_{th}$ = W/L*0.1 μA at V_d = 50 mV), and in the ohmic region by I_d/SQRT(g_m) extrapolation (where g_m is the transconductance) to the intercept with the horizontal axis. The subthreshold slope (S) typically was measured at the drain current range from 10^{-11} A to 10^{-8} A. The mobility of the carriers (μ) was calculated by measurements of the slope (K) of the Id/SQRT(g_m) function in the ohmic region [3]-[4]:

$$\frac{I_d}{\sqrt{g_m}} = K(V_G - V_{th}), \qquad \ldots(1)$$

$$\text{where } K = \sqrt{\frac{\mu V_d C_{ox} W}{L}} \qquad \ldots(2)$$

The measurement included threshold voltage, subthreshold slope, mobility of the charge carriers, effective dimensions, gate leakage current, and investigation of edge effects- as briefly described below. For detailed test results and data plots, refer to full report being posted on the NEPP web site.

3.1 Threshold Voltage

The threshold measurements were made on 15 to 20 transistors of N- and P-type on three dice. Average and standard deviations of the V_{th} values for transistors with the same gate width and length were calculated. Mean value of these characteristics are shown in Table 1. It was observed that variation of the V_{th} within one wafer did not exceed 5% for the P-channel devices. However, characteristics of the front gate channels in the N-channel transistors were less reproducible and the variation reached 12%. The front-gate threshold voltage in P-channel transistors significantly increased with decreasing the channel length from approximately –850 mV at L = 8 μm to 0V at L = 0.2 μm. N-channel transistors manifested similar trend; however, the decrease was much smaller (on the average, from 550 to 420 mV) and scattering of the data was larger.

The scaling effect in SOI FD PMOS transistors is illustrated in Figure 1.

Table 1. Threshold Voltages of FDSOI FETs.

Gate	Mean V_{th}	Std. Dev.	Std. dev/avr, %
N-ch front	560.2 mV	65.8	11.7
N-ch back	8.3 V	0.5	5.7
P-ch front	-609.6 mV	23.2	4.4
P-ch back	-9.4 V	0.2	2.2

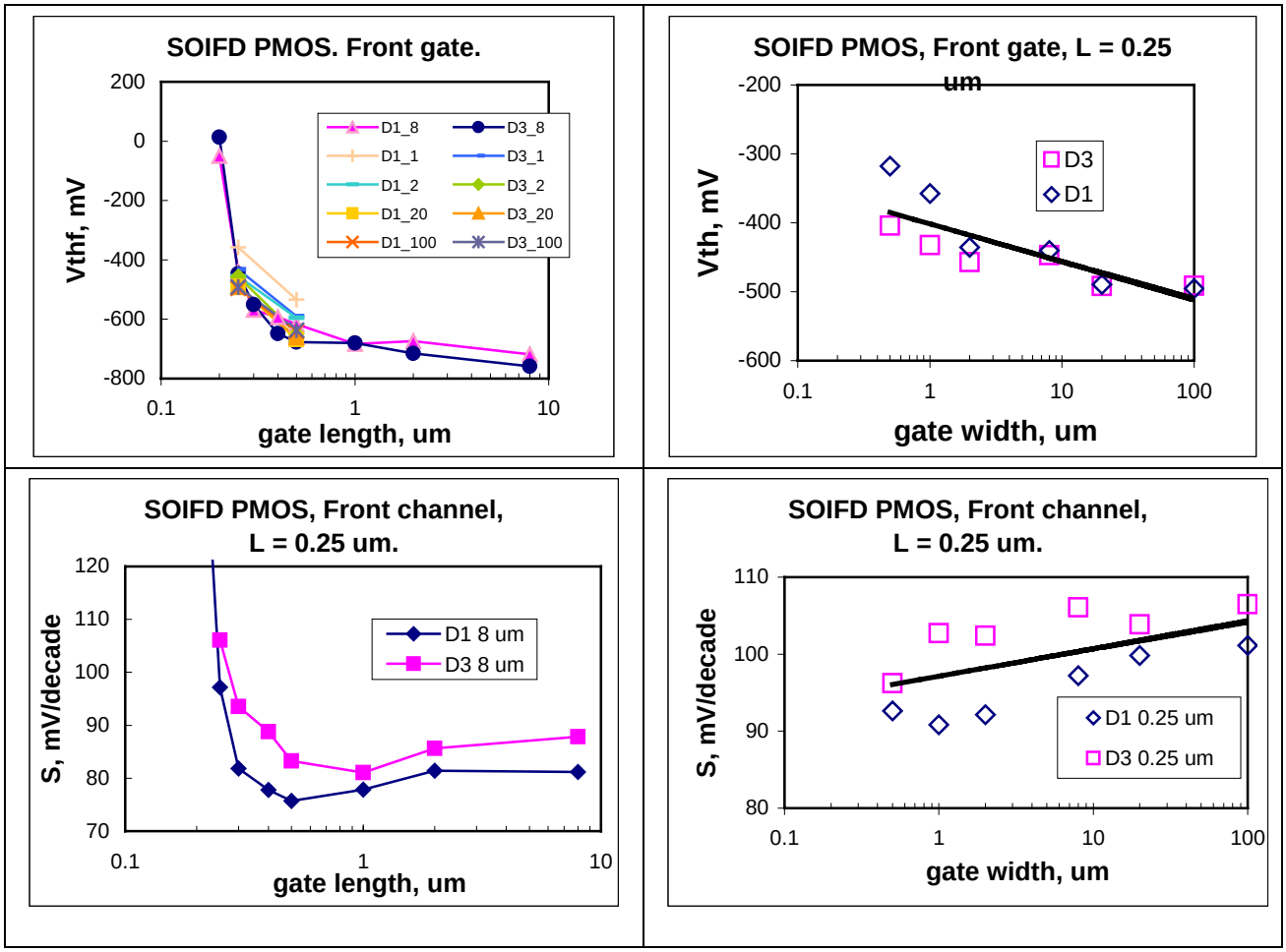

Figure1. Scaling Effects in FDSOI PMOS Transistors.

3.2 Subthreshold Slope

Average subthreshold slope values, their standard deviations, and variations from the calculated minimal values for 0.25 μm process transistors are shown in Table 2. It is seen that the variation of the S values is below ~ 10% except for the back channel in the NMOS transistors, where it reached ~ 20%.

Table 2. Subthreshold Slope (mV/decade)

Gate	average	Std.dev.	(S-Smin)/Smin, %
N-ch front	80	9	29
N-ch back	960	210	91
P-ch front	99	5	60
P-ch back	1110	98	120

3.3 Mobility of Charge Carriers

The front gate mobilities of the charge carriers in transistors of both types were approximately 20-30% less than the volume values, which is usually explained by additional scattering at the Si/SiO_2 interface. The back channel mobility was significantly larger than the front gate mobility.

3.4 Effective Dimensions

The calculations of the transconductnce parameter K (see Eq.2) for transistors with different drawn gate width (W_{mask})and length (L_{mask}) allows estimations of the effective channel length and width, which might deviate from the drawn values. The experimental data showed that in most cases, the gate size deviation from the drawn values is negligible.

3.5 Gate Leakage Current

Attempts to measure gate leakage currents directly showed that they were below the limit of HP4156 sensitivity ($<10^{-13}$ A in the used set up). For this reason, the gate lifting technique was used. The drain current was monitored after applying corresponding bias to contact pads of a transistor, following a mechanical disconnection (lifting) of the gate probe. The drain current decreased with time, indicating a decrease in the gate voltage caused by the oxide leakage current. The drain current declined exponentially and the characteristic time of the decay $\tau = RC$ (where R is the effective resistance of the oxide and C is the capacitance) allowed for calculation of the resistance. The calculations showed that the gate oxide resistance was approximately 2×10^{18} Ohm, which corresponds to negligible leakage currents in the range of femto-amperes

3.5 Edge Effect

A decrease in the gate width significantly increases the possibility that the parasitic conduction path between the drain and source at the lateral edges in SOI MOS FETs would provide a major contribution to the leakage current in the OFF condition of transistors. The side-wall transistor, which is always formed in mesa-isolated structures, operates in parallel with the main transistor and may cause failures of SOI devices.

Analysis of more than 100 different transistors performed in this work did not reveal any excessive leakage currents, which might be related to the edge effect, (except for one case where the current was approximately 10^{-11} A).

4.0 Conclusions

The front- and back-channel N-and P-type transistors manufactured in MIT/LL 0.25 μm SOIFD technology were fully characterized using three process monitor dice with 40 transistors in each die (the gate length varied from 0.2 μm to 8 μm and the gate width varied from 0.5 μm to 100 μm). The test results are summarized below.

- The variations in the threshold voltage and the subthreshold slope did not exceed 12% and 20 % (respectively for V_{th} and S). Characteristics of the front channels in NMOS FETs were much less reproducible than for the PMOS transistors.
- Both N- and P-channel transistors exhibited the short channel effect. The absolute values of the threshold voltage decreased significantly below 0.5 μm.

The effect was most pronounced for PMOS transistors. A decrease in the gate width, also resulted in a decrease of the absolute value of the threshold voltage.

- The subthreshold slope also showed a strong gate-length dependence, significantly increasing in the submicrometer region (more than twice for the back channel, and approximately 15% - 25% for the front channel transistors).
- The mobility of the charge carriers virtually did not change with the gate length for the front-channel NMOS transistors and increased for the PMOS transistors when the gate length decreased below 0.5 μm.
- Electrical measurements showed that the gate length deviations did not exceed 2% of their drawn value.
- The specific resistance of the gate oxide was approximately 10^{15} Ohm*m and the gate leakage current was in the femto-ampere range.
- The parasitic side-wall transistor at the gate edge resulted in some deviations of the transconductance characteristics for the NMOS transistors with the gate width below 2 μm. However, no excessive leakage currents in the OFF condition of the transistors, or any other significant anomalies were observed.

References

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[4] S.Crisoloveanu and S. Li, "Electrical Characterization of SOI Materials and Devices," Kluwer Academic Publishers, 1995.